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Remarks

This Amendment is responsive to the July 18, 2006 Office Action. Reexamination and reconsideration of **claims 1-12, 14-26, and 29-30** is respectfully requested.

Summary of The Office Action

Claims 22, 28, and 29 were rejected under 35 U.S.C. §101 as purportedly being drawn to non-statutory subject matter. Paragraph [0018] has been amended to remove references to the purportedly intangible embodiments (e.g., carrier wave signals), and thus respectfully requests that these rejections be removed. Claim 28 has been cancelled.

Claims 1, 7-11, 13, 14, 18, 21, 22, 23, and 25-30 were rejected under 35 U.S.C. §102(b) as being anticipated by Garrett (U.S. Pat. 6,018,809)(Garrett). Claims 13 and 28 have been cancelled.

Claims 2-6, 15-17, 19, 20 and 24 were objected to as being dependent upon a rejected base claim, but identified as being allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 4, 5, 6, 15, 17, 19, 20, and 24 have been rewritten as appropriate to be in independent form. Claim 16 depends from a claim rewritten in independent form.

Claim 12 has been allowed.

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Objections to Informalities in the Claims

The Examiner's careful review of the claims is greatly appreciated. All of the informalities identified by the Examiner have been corrected in the claims. Applicant does not believe the scope of the claims have been changed since the amendments relate to adding the word "one" to complete the phrase "one or more". No new matter has been added.

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The Claims Patentably Distinguish Over the References of Record

35 U.S.C. §102

For a 35 U.S.C. §102 reference to anticipate a claim, the reference must teach every element of the claim. Section 2133 of the MPEP recites:

> A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Here, the reference does not appear to describe receiving data from both a hardware analyzer and a software analyzer. Instead, the reference appears to describe delivering data to a hardware analyzer and/or a software analyzer. Thus, none of the claims are anticipated by Garrett.

Individual claims will now be discussed.

Independent Claim 1

Claim 1 is directed to a correlating debugger. Claim 1 recites four logics. A first logic receives a first data set from a hardware analyzer. A second logic receives a second data set from a software analyzer. A third logic receives a binding data from either the hardware analyzer or the software analyzer. The binding data facilitates synchronizing the first and second data. A fourth logic receives a signal that an interaction between a hardware device and a software device has occurred and, upon receiving the signal, selectively stores elements of the first data set and the second data set in a time ordered data set.

The Office Action asserts that the capture logic 38 of trace engine 28 discloses the first, second, and third logics. The capture logic 38 clearly receives data from a SCSI bus. Additionally, there can clearly be multiple capture logics 38 in multiple trace engines 28. However, the data captured by the capture logics 38 does not appear to originate at either a hardware analyzer or software analyzer. Instead, the data appears to travel between a host computer (22) and a storage subsystem (24), neither of which is identified or appears to function as either a hardware analyzer or a software analyzer. Instead, the host computer (22) and the storage subsystem (24) appear to function as a conventional computing device

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and a conventional storage subsystem. Neither is performing a hardware analyzing or a software analyzing function. For at least this reason, claim 1 is not anticipated.

Additionally, to the extent that the computer (22) and/or the storage subsystem (24) could be characterized as being a software/hardware analyzer, the selective storing of information based on receiving a signal that an interaction between a hardware device and a software device has occurred appears to be missing in the reference. For this additional reason claim 1 is not anticipated.

Since claim 1 recites features not taught or suggested by the reference, claim 1 patentably distinguishes over the reference. Accordingly, dependent claims 2-3 also patentably distinguish over the reference and are in condition for allowance.

Dependent Claims 2-3, 7-11

These claims depend from claim 1. Thus, the arguments above apply equally to these claims. Accordingly, these dependent claims distinguish over the reference and are in condition for allowance.

Claim 7

This claim depends from claim 1, which has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, this claim recites that the signal received by the fourth logic is a non-maskable interrupt. The reference describes generating an interrupt when a trace buffer 34 approaches its capacity. Generating an interrupt when a buffer is full does not anticipate determining when to begin storing data based on receiving a non-maskable interrupt. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 10

This claim depends from claim 1, which has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, this claim recites that the software component and processor executable instructions associated with the first logic, second logic, third logic, and/or fourth logic all run on a first processor. The reference describes trace

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engines and capture logics that run on a system connected to a bus between a computer and a storage device. The reference does not appear to disclose an embodiment where the trace engines and capture logic run inside either the computer or the storage device. For this additional reason this claim is not anticipated and is in condition for allowance.

Claim 11

This claim depends from claim 1, which has been shown to be not anticipated. Thus, this claim is similarly not anticipated. Additionally, this claim recites that the software analyzer from which the second data set is received is a kernel debugger. The reference describes the receiving component (e.g., trace analyzer 30) being a kernel debugger. Delivering received information to a kernel debugger does not anticipate receiving information from a kernel debugger. For this additional reason this claim is not anticipated and is in condition for allowance.

Independent Claim 14

Claim 14 is directed to a method associated with a correlating debugger. Claim 14 recites six actions: establishing a relationship in a debugger between a hardware device and a software component that will perform a software operation related to the hardware device; configuring a software analyzer; configuring a hardware analyzer; detecting a first event associated with the a software operation; detecting a second event associated with a hardware operation; and selectively storing data from the software analyzer and the hardware analyzer.

The Office Action asserts that multiple trace engines are synchronized. This appears to be correct. The Office Action also asserts that a software analyzer is configured to collect data from a software component and to deliver that data to the debugger. Similarly the Office Action asserts that a hardware analyzer is configured to collect data from a hardware device and to deliver that data to the debugger. While both hardware data and software data may be collected of the SCSI bus, this data is not coming from either a hardware analyzer or a software analyzer. The data is coming from either host computer 22 or storage subsystem 24, neither of which is performing a hardware analyzing or a software analyzing function. For at least this reason, claim 14 is not anticipated.

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Additionally, to the extent that host computer 22 or storage subsystem 24 could be described as being a hardware analyzer or a software analyzer, none of the trace engines 28 configure the host computer 22 or the storage subsystem 24. Thus, even if the Office Action is correct that data is received from a hardware analyzer and a software analyzer, the claimed element of configuring the hardware analyzer and the software analyzer is not present. For this additional reason this claim is not anticipated.

Claim 18

Claim 18 depends from claim 14, which has been shown to be not anticipated and thus this claim is similarly not anticipated. Additionally, claim 18 further characterizes how a hardware analyzer is configured. Since the reference does not disclose configuring a hardware analyzer from which a correlating debugger can receive data, it follows that the reference also does not further characterize how the hardware analyzer will be configured. For this additional reason this claim is not anticipated and is in condition for allowance.

Independent Claim 23

Claim 23 describes a method that includes engaging both a hardware analyzer and a software analyzer and then binding the two together. While the reference describes synchronizing data, and may even describe that the data may be either hardware data or software data, the reference does not describe that the data is received from a hardware analyzer and a software analyzer. Any data received by the trace engines described in the reference will be received off a SCSI bus between a host computer 22 and a storage subsystem 24. Thus the data will be from neither a software analyzer nor a hardware analyzer. For at least this reason this claim is not anticipated and is in condition for allowance.
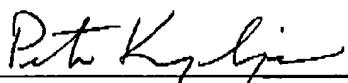
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Conclusion

For the reasons set forth above, **claims 1-12, 14-26, and 29-30** patentably distinguish over the references and are allowable. An early allowance of all claims is earnestly solicited.

Respectfully submitted,

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